21. (twice amended) A method of debugging a ~~processor, said~~ method comprising:

a) providing information about processor activity in real time; and

b) associating the instructions executed by the processor with the information about processor activity, wherein

[said step of providing information about processor activity includes providing information about every instruction executed by the processor].

said step of providing information about processor activity includes providing information that the processor has not executed an instruction during the last processor cycle.

23. (amended) A method according to claim [22] 21, wherein:

[said step of providing information about processor activity includes providing information that the processor has not executed an instruction during the last processor cycle]

said step of providing information about processor activity includes providing information about every instruction executed by the processor.

Kindly add new claims 26 and 27 as follows.

26. A processor having a real time debugging interface, said processor comprising:

a) instruction memory means for storing instructions to be executed by said processor;

b) program counter means coupled to said instruction memory means for indexing said instructions;

c) cause register means for indicating information regarding interrupts and exceptions; and

d) first decoder means for indicating information about an instruction executed by said processor during a clock cycle, said first decoder means being coupled to said instruction memory means, said program counter means, and said cause register means, said first decoder means having a first output, wherein

said first output provides information regarding activity of said processor in real time,

said clock cycle is a processor clock cycle,

said first decoder means updates said information about each instruction executed by said processor for each said processor clock cycle, and

said information about each instruction executed by said processor includes an indication whether or not an instruction has been executed since the previous processor cycle.

27. An embedded system having a plurality of processors and a real time debugging interface, said system comprising:

a) a plurality of instruction memory means for storing instructions to be executed by a respective one of said plurality of processors;

b) a plurality of program counter means, each coupled to a respective one of said plurality of instruction memory means for indexing contents of said instruction memory means;

c) a plurality of cause register means for indicating information regarding interrupts and exceptions for a corresponding one of said plurality of processors, each of said cause register means being coupled to a respective one of said processors; and

d) a plurality of first decoder means, each said first decoder means coupled to a respective one of said instruction memory means, to a respective one of said program counter means, and a respective one of said cause register means, each said first decoder means for indicating information about an instruction executed during a clock cycle by a respective one of said processors, each said first decoder means having a first output, wherein

each said first output provides information regarding activity of said processor in real time,

said clock cycle is a processor clock cycle,

each said first decoder means updates said information about each instruction executed by a respective processor for each said processor clock cycle of said respective processor, and

each said information about each instruction executed by a respective processor includes an indication whether or not an instruction has been executed since ~~the~~ a previous processor cycle of said respective processor.

REMARKS

The Applicants appreciate the Examiner's cooperation in the telephone interview of February 25. During the interview it was agreed that if the claims were amended to state "directly coupled" rather than merely "coupled", they would define over the art of record. It is the understanding of the undersigned that the word "connected" is typically used to mean directly coupled whereas the word "coupled" allows for intermediate elements between the elements which are "coupled". Therefore, the claims have been amended to change the word "coupled" to the word "connected". It is submitted that this is the same as "directly coupled".

New claims 26 and 27 correspond to original claim 4 and 14 which the Examiner has indicated as being allowable.

In light of all of the above, it is submitted that the claims are in order for allowance, and prompt allowance is earnestly